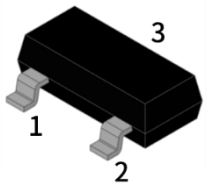
DTA114ECALST1

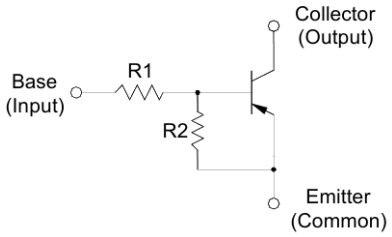
PNP Silicon Epitaxial Planar Digital Transistor

1. FEATURES

- With built-in bias resistors.
- Simplify circuit design.
- Reduce a quantity of parts and manufacturing Process.



SOT23 (TO-236)



2. Mechanical Data

- SOT-23 Small Outline Plastic Package.
- Tin plated leads, solderable per J-STD-002 and JESD22-B102.
- Marking: 14

3. ORDERING INFORMATION

Device	Min Pack	Inner Box	Outer Carton	Reel
DTA114ECALST1	3000	45000	180000	7 inch

4. MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Supply Voltage	VCC	-50	V
Input Voltage	VIN	-40 ~ +10	V
Output Current	IO	-50	mA
Peak Collector Current	ICM	-100	mA
Total Device Dissipation	PD	200	mW

5. THERMAL CHARACTERISTICS

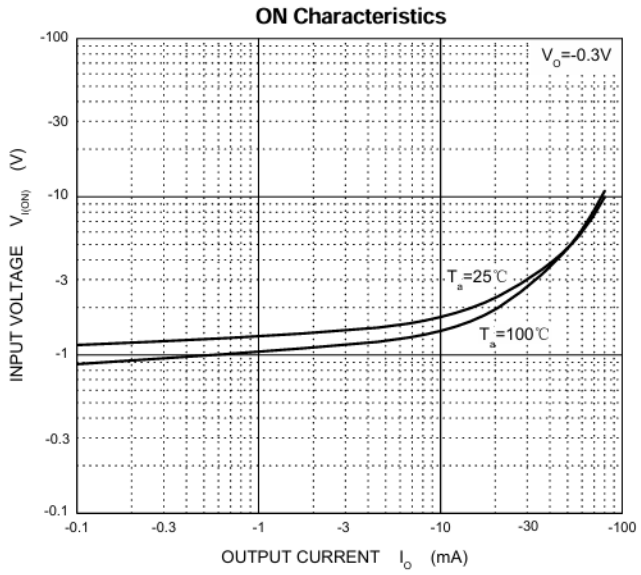
Parameter	Symbol	Limit	Unit
Junction Temperature	TJ	150	°C
Storage Temperature	TSTG	−55~+150	°C

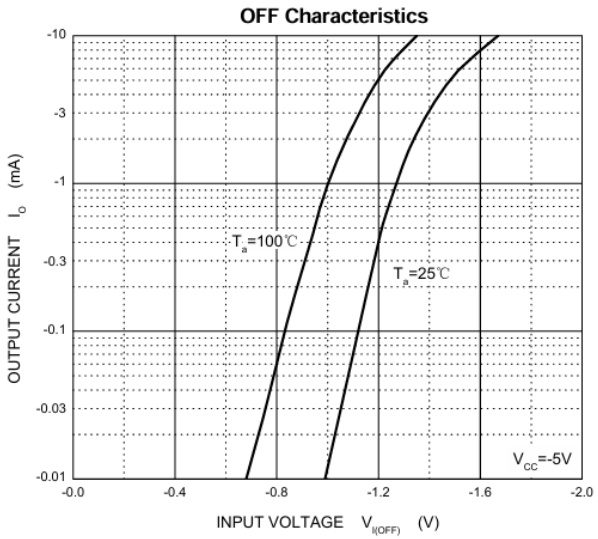
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C unless otherwise specified)

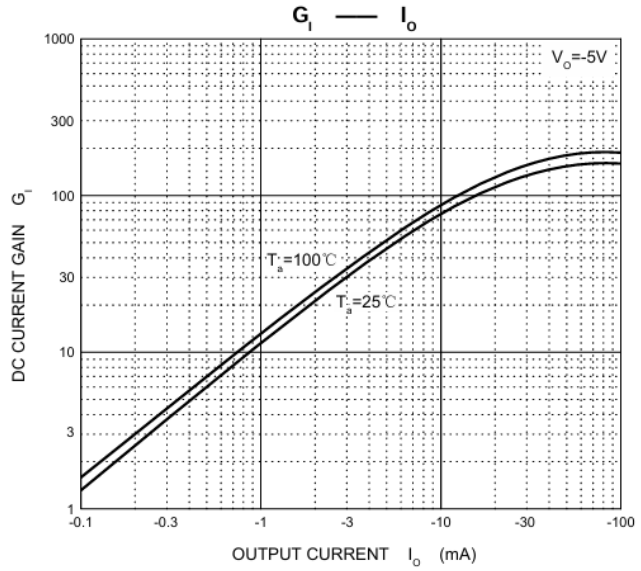
Parameter	Symbol	Condition	Min	TYP	Max	Unit
Input Voltage	VI(off)	V =-5V,IO=-100μA	-0.5			V
	VI(on)	V=-0.3V,IO=-10 mA			-3	V

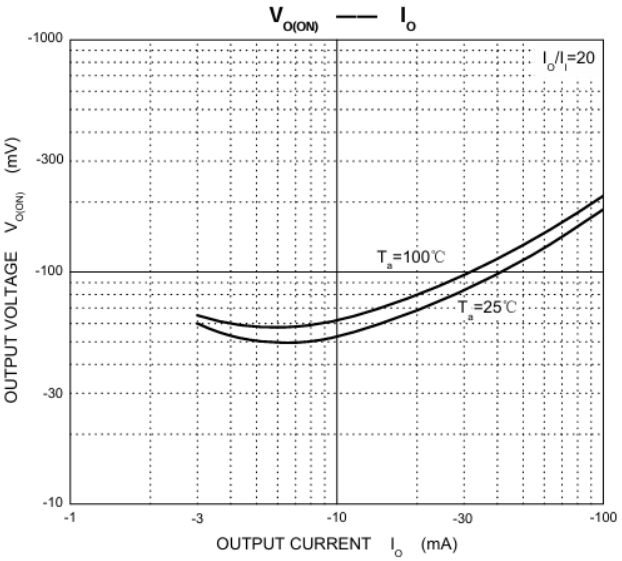
Output voltage	VO(on)	IO/Ii=-10mA/-0.5mA			-0.3	V
Input current	Ii	VI=-5V			-0.88	mA
Output current	IO(off)	VCC =-50V,VI=0			-500	mA
DC current gain	GI	VO=-5V,IO=-5mA	30			
Input resistance	R1		7	10	13	kΩ
Resistance ratio	R2/R1		0.8	1	1.2	
Transition frequency	fT	VO=10V, IO=-5mA,f=100MHz		250		MHz

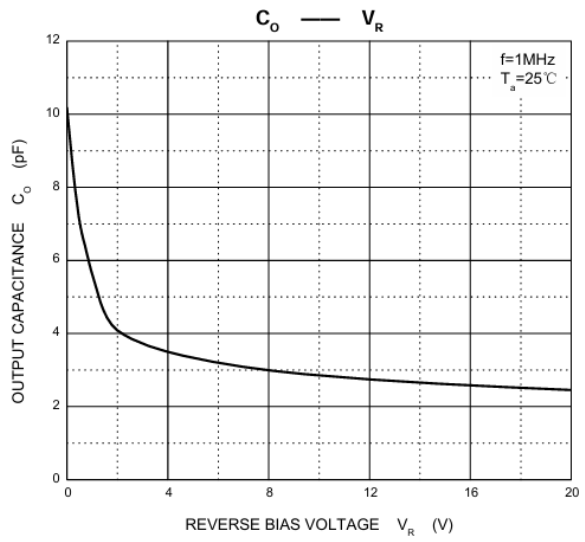
7. ELECTRICAL CHARACTERISTICS CURVES

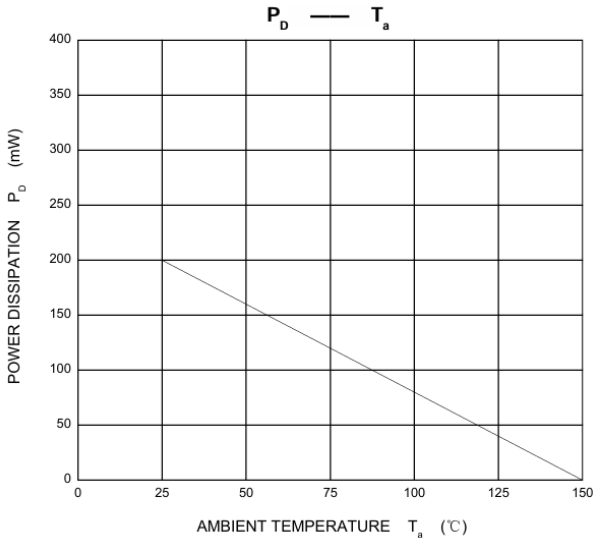




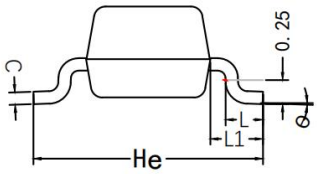


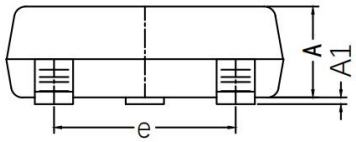


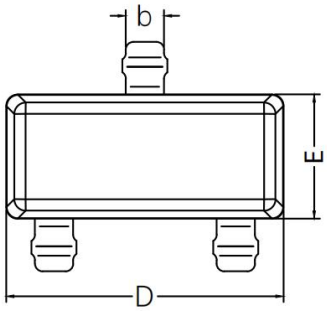




8. OUTLINE AND DIMENSIONS

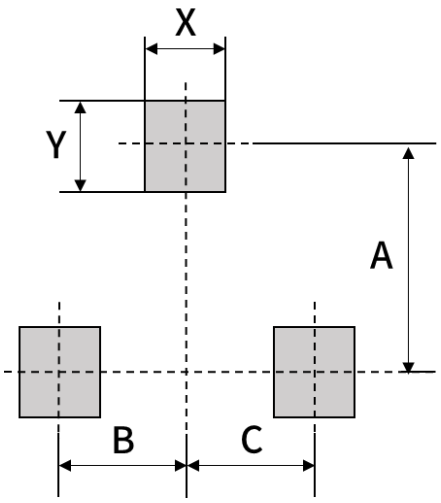






DIM	MIN	NOR	MAX
A	0.85	0.95	1.05
A1	0.01	0.06	0.10
b	0.36	0.44	0.52
c	0.09	0.13	0.18
D	2.80	2.90	3.10
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.40	0.50
L1	0.35	0.50	0.65
He	2.10	2.35	2.50
θ	0°	-	10°
All Dimensions in mm			

9. SUGGESTED PAD LAYOUT



SOT23		
DIM	mm	inch
A	2.00	0.079
B	0.95	0.037
C	0.95	0.037
X	0.80	0.031
Y	0.90	0.035

10. DISCLAIMER

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